The European Proceedings of
Social and Behavioural Sciences
EpSBS

www.europeanproceedings.com
e-ISSN: 2357-1330

DOI: 10.15405/epsbs.2024.10.40

SCTMG 2023
International Scientific Conference «Social and Cultural Transformations in the Context of Modern Globalism»

MULTILAYER ECO-FRIENDLY COMPOUNDS FOR COMPLEX ENVIRONMENTALLY SAFE STRUCTURES

Gasan A. Mustafaev (a)*, Arslan G. Mustafaev (b), Adlan I. Khasanov (c)
*Corresponding author

(a) Kabardino-Balkarian State University, 173, st. Chernyshevsky, Nalchik, 360004, Russia; arslan_mustafaev@mail.ru
(b) Dagestan State University of National Economy, 5, st. J. Atayeva, Makhachkala, 367008, Russia
(c) Chechen State University, 32, st. A. Sheripova, Grozny, 364024, Russia; Grozny State Oil Technical University, 100, avenue Kh. Isaeva, Grozny, 364051, Russia

Abstract

The formation of highly reliable multilayer metallization systems is one of the priority tasks of modern microelectronics. In this work, thin-film layers of interconnects separated by polyimide layers are studied. A multilayer ceramic or silicon substrate was used as the upper layer of the interconnects. The resulting structure, interconnecting a large number of VLSI chips, makes it possible to reduce delays, power consumption and noise levels. Multilayer thin-film structures were formed by irradiating the photoresist, followed by reactive ion etching, then pattern formation, and electron-beam evaporation. Three-layer films of chromium-copper-chromium are used as conductors, copper is chosen as a good electrical conductor, its conductivity is much higher than that of aluminum or aluminum-copper alloys. In order to avoid interaction of copper with polyimide and acids during the manufacturing process, chromium was chosen as a passivating metal. Crystals with rows of conductor lines were fabricated, on which the resistance of the Cr-Cu-Cr metallization system was measured using the four-probe method. The technology for manufacturing holes in multilayer interconnects of multichip integrated circuits and metallization parameters that give the best results are experimentally determined.

Keywords: Aluminum-copper alloys, conductor lines, integrated circuits, metallization system, multilayer metallization systems, reliable

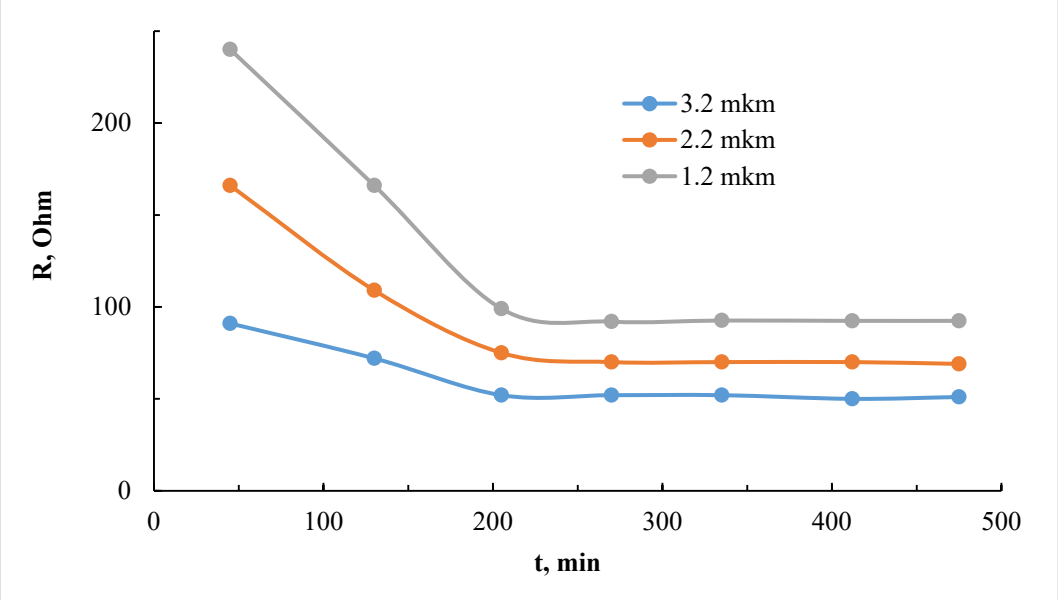
https://doi.org/10.15405/epsbs.2024.10.40
Corresponding Author: Gasan A. Mustafaev
Selection and peer-review under responsibility of the Organizing Committee of the conference
eISSN: 2357-1330

1. Introduction

As the technology of integrated circuits improves, the density of components on them increases, which results in scaling of the component size and, accordingly, a decrease in the thickness and width of metallization strips, as well as in an increase in the number of metallization segments. The transition to very large scale integration circuits (VLSI) toughen the requirements to metallization parameters that determine its reliability, such as contact resistance, the quality of step coating, the number and size of stress-induced voids, and electromigration resistance.

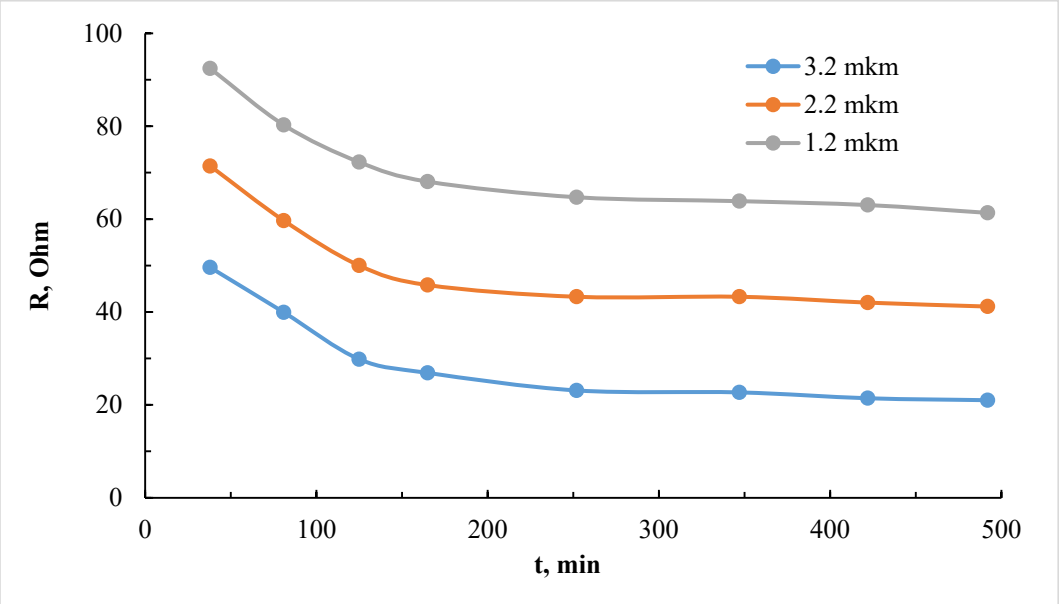
2. Problem Statement

As a rule (Geipel et al., 2016; Song et al., 2005; Tan & Roy, 2007), an aluminum-silicon alloy is used for metallization; its additives prevent the breakdown in shallow junctions. However, during the cooling process, silicon dissolved in aluminum can be separated from a solid solution with aluminum. In such case, silicon precipitates may be formed at nucleation sites, such as pre-existing silicon particles, grain boundaries in an aluminum film or steps in a dielectric, and epitaxial deposition may also occur on the exposed areas of the substrate (Giza, 2024; Mambetova et al., 2024; Mascareno & Chavez, 2024). With a decrease in the size of the contact hole, the proportion of the area occupied by the resulting epitaxial layer becomes significant, resulting in a sharp increase in contact resistance. Figure 01 shows the dependence of the contact resistance on the annealing time for n+ and p+ of -epitaxial layers, respectively, on the metallization of Al-Si (1%) after annealing at 450 °C. In this case, the contact ceases to be ohmic, which leads to a nonlinear dependence of the device parameters on the power source voltage.



(a)

https://doi.org/10.15405/epsbs.2024.10.40
Corresponding Author: Gasan A. Mustafaev
Selection and peer-review under responsibility of the Organizing Committee of the conference
eISSN: 2357-1330



(b)

Figure 1. The contact resistance dependence on the annealing time for different sizes of contact hole diameters for: a) n^+ and b) p^+ of epitaxial layers

3. Research Questions

One of the most common types of aluminum-based metallization failures are circuit breaks during thermal cycling caused by void formation. Void formation is caused by mechanical stresses that occur when the plate is cooled after applying a passivating layer of silicon oxide or nitride. Stresses gradients cause the vacancies diffusion and their subsequent coalescence with the formation of voids, which occurs mainly at the edges of the lines. The criticality of this process increases as the width of the metallization line decreases (Collet-Sabé, 2023; Manakbayeva, 2023; Sheveleva, 2024). The suppression of voids formation is facilitated by the introduction of copper into aluminum and the application of an underlayer of some refractory materials, for example, molybdenum silicide. Voids also induce failures in through-holes at the boundary of two layers of metals. The refractory metal application before the precipitation of the second metallization layer prevents the spread of voids into aluminum from the interface of two metallization layers.

4. Purpose of the Study

The placement of an additional metal layer between the aluminum film and the contact contributes to the prevention of epitaxial precipitation. This layer should provide minimal interaction with aluminum, not affect other properties of the film and have a low contact resistance with both n+ and p+ zones. Such requirements are met by silicides of molybdenum, tantalum and tungsten, an alloy of titanium with tungsten and titanium (Gan et al., 2003; Meng et al., 2008; Patra et al., 2023). Thus, the introduction of a layer of tungsten silicide made it possible to maintain a low contact resistance of a contact with a diameter of 1.2 microns at a temperature of up to 450 °C, while without this layer the contact resistance increased distinctly.

https://doi.org/10.15405/epsbs.2024.10.40
Corresponding Author: Gasan A. Mustafaev
Selection and peer-review under responsibility of the Organizing Committee of the conference
eISSN: 2357-1330

5. Research Methods

The quality of aluminum film, the surface of which is very sensitive to contamination of dielectric layer, is improved by the preliminary deposition of a layer of a refractory compound (for example, an alloy of tungsten with titanium, titanium nitride or pure titanium). Such an underlayer provides a more reproducible deposition of the aluminum film than a low-temperature oxide does. Experiment (Alam et al., 2005) shows that under conditions of constant displacement, the electromigration (EM) resistance of the aluminum film sharply decreases. The refractory material underlayer application is desirable in order to prevent aluminum peeling-off. It is also proposed to act on the deposited aluminum layer by pulsed UV laser radiation; the molten metal flows down the walls of the step and enters the through-hole. To minimize the interaction of aluminum with the underlying layers, the pulse duration should be about 10 ns (Mele, 2022; Nikulin, 2023; Rawel, 2022). The presence of a TiW underlayer and high initial temperature of silicon slice make aluminum melting possible at low laser radiation power. The use of Al-Si (1%) alloy as the top layer of complementary metal-oxide-semiconductor metallization, planarization by laser radiation, facilitates photolithography; at the same time, such advantages inherent in this metallization system as insignificant mutual diffusion with an underlayer of refractory material and electromigration resistance are preserved (Tan & Roy, 2007).

6. Findings

EM can lead to failure when passing a high-density current through metallization and is becoming increasingly critical for VLSI complementary metal-oxide-semiconductor, as higher excitation currents and synchronization frequencies of logic metal-oxide-semiconductor integrated circuit are used. The improvement of metallization resistance to EM is achieved by adding 4% copper to aluminum, however, for submicron circuits, the copper content cannot exceed 2% when using dry etching methods (Kudo et al., 2021; Yan et al., 2019). The titanium introduction facilitates etching, but this metal contributes to voids formation (Tan & Roy, 2007). A significant improvement in EM resistance is provided due to the placement of an aluminum film between two TiW layers: the lower layer shunts the current in the event of voids being formed in the aluminum layer (Meng et al., 2008). In such metallization, the failure mechanism may consist in lateral extrusion, which will eventually lead to a chain break. Planarization by a dielectric layer helps to reduce the likelihood of extrusion. EM can occur not only in metallization but also in contacts and through-holes. This leads to fluctuations in the thickness of the aluminum layer on side walls of the hole and, consequently, it results in a decrease in its ability to conduct current. As for thermal stresses, the zone of interface between two layers of metal in a through-hole is vulnerable in terms of EM resistance. The quality of metallic aluminum in holes depends on the deposition rate on the walls, as well as the presence of impurities on them remaining after etching the hole. In this regard, EM can be considered as the best way to check the quality of metallization. Studies have shown that for this metallization system there is a direct relationship between its resistance to stress-induced voids and a tendency to EM. The experimental results suggest that geometric factors play a dominant role in the mechanism of metallization destruction of integrated circuits due to electromigration. The increasing current density during metallization because of the fact that when voids are formed, its effective cross-

https://doi.org/10.15405/epsbs.2024.10.40
Corresponding Author: Gasan A. Mustafaev
Selection and peer-review under responsibility of the Organizing Committee of the conference
eISSN: 2357-1330

section decreases, leads to an increase in the metallization temperature in local areas. This results in an acceleration of bubbles growth, in an acceleration of electromigration as well as relatively quickly can cause breakages of metallization.

Very large scale integration circuits have metallization lines less than 0.1 microns wide. Studies have shown (Jang et al., 2003; Yu et al., 2007) that the migration of material under the influence of mechanical stresses at sizes commensurate with the grain size accelerates, the failure rate increases, and at the same time the average time to failure decreases due to electromigration with a decrease in the width of metallization.

Trends in integrated circuits development lead to the creation of multi-chip circuits equipped with multilayer interconnects with a high density of conductors. Thin-film layers of interconnects are separated from each other by thin layers of polyimide with a small dielectric constant. The top layer of these interconnects is a multilayer ceramic or silicon substrate. Such a structure, connecting a large number of VLSI crystals, makes it possible to reduce delays, reduces power consumption, and noise level. Multilayer thin-film structures are produced by photoresist illumination, reactive ion etching, template formation and electron beam evaporation. Three-layer chromium-copper-chromium films are used as conductors, copper is chosen as a good electrical conductor, its conductivity is much higher than that of aluminum or aluminum-copper alloys. To avoid the interaction of copper with polyimide and acids during production, a passivating metal was chosen, chromium in the form of a thin film (less than 20 nm) protecting copper conductor. The passivating metal surrounds the copper conductor, protecting it from the effects of acids.

Crystals were made with rows of conductor lines, on which there was measured the resistance of chromium-copper-chromium lines made using the same technology as the lines on the interconnects. Reactive etching was carried out in a mixture of 2% CF4-O2. The thickness of lines is 5–20 nm /0.8–1 microns / 5–0 nm, the resistance of three-layer lines of metallization is between 1.75 and 1.95 mcOm-cm. The minimum resistance values were obtained during the formation of lines at a substrate temperature of 150 °C, higher resistances were obtained at a lower substrate temperature during line formation. Annealing at elevated temperature led to a decrease in metallization resistance, eliminating such structural defects as vacancies, dislocations, grain boundaries in copper. Reactions occurring in metallization, in polyimide layers during the fabrication of metallization, at different stages of fabrication process have been studied. Table 01 shows the change in the resistance of metallized films of different compositions at different annealing temperatures. When using palladium, platinum and nickel, during annealing, these elements diffuse into copper, significantly increasing the metallization resistance. With an increase in temperature, the intensity of penetration of these metals into copper increases, and in the metallization of Cr-Cu-Cr, chromium practically does not diffuse into copper, even at maximum temperature, which explains the stability of resistance in this metallization system.

https://doi.org/10.15405/epsbs.2024.10.40
Corresponding Author: Gasan A. Mustafaev
Selection and peer-review under responsibility of the Organizing Committee of the conference
eISSN: 2357-1330

Table 1. Change in the resistance of metallized films of different composition at different annealing temperatures

Film composition	Film resistance, 10^{-3} Om/□	Change in resistance after annealing, %		
		150°C	300°C	400°C
Cr/Cu/Cr	8.3	-1	-2	-2
Cr/Cu/Pd	9.7	-2	+10	+25
Cr/Cu/Pt	9.3	-2	+11	+32
Cr/Cu/Ni	10.6	-1	+7	+43
Cr/Cu/NiB	9.8	-1	-2	+31

The measurements were carried out by the four-probe method at current values of 5, 10, 15, 20 and 25 mA. The presence of ohmic contact in the metallization of holes is confirmed by the linear voltage characteristic.

The influence of etching process on holes formation and reliability of metallization of holes have been evaluated. Studies have shown that the resistance levels of metallization of holes depend on many variables of the technological process. Table 02 shows the values of resistances for holes with a diameter of 2 and 3 microns, depending on the thickness of upper and lower chromium layers, with different types of etching.

Table 2. Hole resistances, depending on the thickness of upper and lower chromium layers

Thickness of top layer, nm	Thickness of lower layer, nm	Metallization resistance, 10^{-3} ohms	
		2 microns	3 microns
5	5	2.63	3.35
5	30	2.71	3.34
10	5	2.59	3.20
10	30	2.67	3.29
20	5	2.75	3.31
20	15	2.70	3.26
20	30	2.78	3.38

7. Conclusion

Thus, the optimal metallization for interconnects is Cr-Cu-Cr metallization. The metallization parameters that give the best results have been experimentally established. There has also been determined the technology of manufacturing holes in multilayer interconnects of multi-chip integrated circuits.

References

Alam, S. M., Wei, F. L., Gan, C. L., Thompson, C. V., & Troxel, D. E. (2005). Electromigration Reliability Comparison of Cu and Al Interconnects. *Sixth International Symposium on Quality of Electronic Design* (ISQED'05). https://doi.org/10.1109/isqed.2005.51

Collet-Sabé, J. (2023). Pre-modern epistemes inspiring a new Global Sociology of Education Imagination. *British Journal of Sociology of Education*, *44*(8), 1249-1266.

Gan, Z., Tan, C. M., & Zhang, G. (2003). Nondestructive void size determination in copper metallization under passivation. *IEEE Transact. on Device and Mater. Reliability, 3*, 69–78.

Geipel, T., Kumm, J., Moeller, M., Kroely, L., Kraft, A., Eitner, U., Wolf, A., Zhang, Z., & Wohlfahrt, P. (2016). Low-temperature Interconnection of PVD-Aluminium Metallization. *Energy Procedia, 98*, 125-135. https://doi.org/10.1016/j.egypro.2016.10.088

Giza, A. (2024). Sociology and the Alienation of Knowledge. *Rethinking the Social*, 15-36. https://doi.org/10.1163/9789004708549_003

Jang, S.-Y., Wolf, J., Ehrmann, O., Gloor, H., Schreiber, T., Reichl, H., & Paik, K.-W. (2003). CrCu based UBM (under bump metallization) study with electroplated Pb/63Sn solder bumps - interfacial reaction and bump shear strength. *IEEE Transactions on Components and Packaging Technologies, 26*(1), 245-254. https://doi.org/10.1109/tcapt.2002.807591

Kudo, H., Haneda, M., Ohtsuka, N., Tabira, T., Sunayama, M., Ochimizu, H., Sakai, H., Owada, T., Kitada, H., & Nara, Y. (2021). Ultrathin Barrier Formation Using Combination of Manganese Oxide Encapsulation and Self-Aligned Copper Silicon Nitride Barriers for Copper Wiring in Future LSI Interconnects. *IEEE Transactions on Electron Devices, 58*(10), 3369-3378. https://doi.org/10.1109/ted.2011.2162959

Mambetova, A., Burganova, R., Tabyldiyeva, O., & Tolepbergenova, A. (2024). The influence of the social well-being of the population on the sustainable development of the region. *E3S Web of Conferences, 537*, 02027. https://doi.org/10.1051/e3sconf/202453702027

Manakbayeva, A. B. (2023). Formation of Personal Moral Values in Complex Social Systems. *Lecture Notes in Networks and Systems*, 887-899. https://doi.org/10.1007/978-3-031-23856-7_76

Mascareno, A., & Chavez, J. M. (2024). Quasi-Sovereignty: *Hobbes, Luhmann, and World Society, 50*, 19–36.

Mele, V. (2022). Metropolis and Modernity. *Marx, Engels, and Marxisms*, 33-59. https://doi.org/10.1007/978-3-031-18184-9_2

Meng, Q., Zhang, J., Li, Z., Li, G., & Chen, R. (2008). Synthesis of molybdenum silicide by both ion implantation and ion beam assisted deposition. *Applied Surface Science, 254*(9), 2678-2684. https://doi.org/10.1016/j.apsusc.2007.10.017

Nikulin, A. (2023). Globalization and the Principles of Tolerance. *Springer Geography*, 152-158. https://doi.org/10.1007/978-3-031-20620-7_14

Patra, S., Chen, D., & Geiger, R. (2023). Reliability degradation with electrical, thermal and thermal gradient stress in interconnects. 2013 *IEEE International Symposium on Circuits and Systems* (ISCAS2013). https://doi.org/10.1109/iscas.2013.6572033

Rawel, J. (2022). An allergy of society: on the question of how a societal “lockdown” becomes possible. *Kybernetes, 51*(5), 1814–1832.

Sheveleva, D. A. (2024). Problems of intercultural dialogue in modern society: finding solutions. *Chelovek, 35*(2), 69-86. https://doi.org/10.31857/s0236200724020043

Song, S., Liu, Y., Mao, D., Ling, H., & Li, M. (2005). Diffusion barrier performances of thin Mo, Mo-N and Mo/Mo-N films between Cu and Si. *Thin Solid Films, 476*(1), 142-147. https://doi.org/10.1016/j.tsf.2004.09.046

Tan, C. M., & Roy, A. (2007). Electromigration in ULSI interconnects. *Materials Science and Engineering: R: Reports, 58*(1-2), 1-75. https://doi.org/10.1016/j.mser.2007.04.002

Yan, H., Tay, Y. Y., Liang, M. H., Chen, Z., Ng, C. M., Pan, J. S., Xu, H., Liu, C., & Silberschmidt, V. V. (2019). Amorphous metallic thin films as copper diffusion barrier for advanced interconnect applications. *2009 11th Electronics Packaging Technology Conference*. https://doi.org/10.1109/eptc.2009.5416485

Yu, M., Zhang, J., Li, D., Meng, Q., & Li, W. (2007). Metal vapor vacuum-arc ion implantation effects on the adhesion and hardness of ion-beam deposited Cr/Cu films. *Applied Surface Science, 253*(6), 3276-3283. https://doi.org/10.1016/j.apsusc.2006.07.019